



INTEGRATED TEST BUS

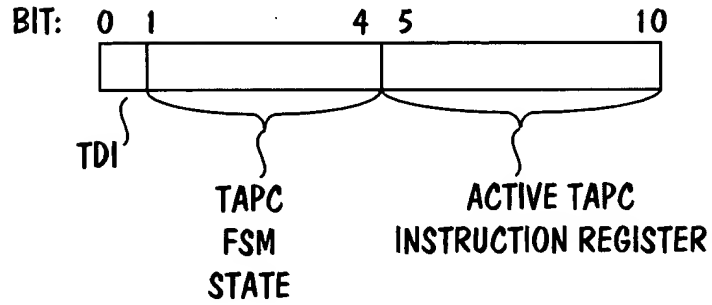


FIG. 6

TAP CORE CONFIGURATION REGISTER

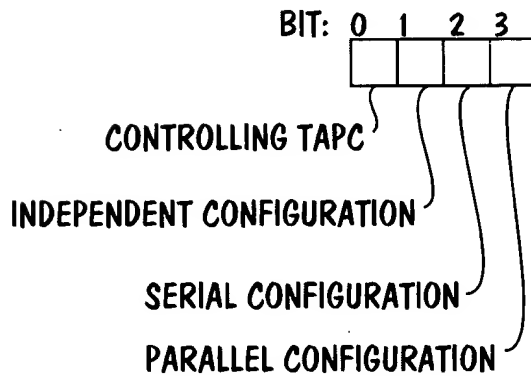


FIG. 7